REMARKS

Claims 1-13 and 17-22 are pending.

Claims 1-4, 9-11, 13, and 17-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,834,782 to Schick et al. in view of U.S. Pat. No. 6,396,539 to Heller et al. Applicants respectfully request reconsideration of this rejection.

Claim 1 recites a CMOS image sensor circuit comprising, *inter alia*, a chip including an "image sensor portion having a first area *and* a second area." The chip is formed to have "at least a first set of parallel edges including a first edge and a second edge," and "a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge." The image sensor portion includes "imaging pixels extending between said first edge, said second edge, and said third edge, such that imaging pixels of said first area of said image sensor portion are adjacent said first edge and said third edge of said chip," and "imaging pixels of said second area of said image sensor portion are adjacent said second edge and said third edge of said chip."

Schick et al. discloses a large-area image detector. An object of the invention disclosed by Schick et al. is "to minimize blind spots in the image." See Schick et al., col. 3, lines 13-15. Schick et al. teaches that invention objectives are achieved using sensors with an active area at a first end of the sensor, and an inactive region. The active area of one sensor is disposed in front of the inactive regions of another sensor. Consequently, light falls only on the active area of each sensor. Light is blocked from striking the inactive region by that portion of the active area which overlaps inactive region. Light does not fall on inactive regions of the sensors, so the objective "to minimize blind spots in the image" is achieved.

The Office Action contends that Schick et al. teaches one of skill in the art to divide the active area of each sensor with a column of drive transistors. Moving the

column of drive transistors away from the sensor edge, discussed in Schick et al. at col. 5, lines 14-20, decreases the width of the inactive region at the edge. Applicants note, however, that a column of drive transistors dividing the active area would create blind spots in the image. As noted in the Office Action, this would create a "central inactive area." A primary objective of Schick et al., however is to "minimize blind spots in the image," as noted above. Thus, Schick et al. teaches directly away from moving the column of drive transistors away from the edge of the sensor. Instead, Schick et al. would teach one of skill in the art that the column of drive transistors should remain near the edge as part of the inactive region. As a result of the Schick et al. overlapping arrangement of sensors, the inactive region of each sensor does not receive light. Consequently, Schick et al. teaches that the inactive region, which can be of any width, should be located along the edge, where it will not create blind spots. Schick et al. does not teach or suggest a CMOS image sensor having a chip with "an image sensor portion having a first area and a second area."

Heller et al. does not cure the deficiencies of Schick et al. Heller et al. has been cited to provide on-chip pixel interpolation, which the Office Action admits is missing from Schick et al. Heller et al. has a single sensor array 12, however, and so does not provide the missing feature of "an image sensor portion having a first area and a second area."

Accordingly, claim 1 is patentable over the proposed combination of Schick et al. and Heller et al. Claims 2-7 and 19-21 depend directly or indirectly from claim 1, and so are patentable for at least the same reasons.

Claim 9 recites a CMOS imager comprising, *inter alia*, a first CMOS image sensor chip having "a control portion and a centralized row-local control portion." The centralized row-local control portion is "physically located inside said image sensor portion in place of a plurality of pixels of the array forming said CMOS image sensor portion," and thereby forms "at least two image sensor areas." As noted above with respect to claim 1, Schick et al. does not teach or suggest an image sensor portion with "at least two image sensor areas." Heller et al., also having a monolithic image sensor portion, does not cure

the deficiencies of Schick et al. Claim 9, and its dependent claim 10, are patentable over the proposed combination of Schick et al. and Heller et al.

Claim 11 recites a method of making a CMOS imager comprising, *inter alia*, "fabricating at least two CMOS image sensor chips having an image sensor portion arranged in an array of rows and columns," "each having a control portion and a centralized row-local control portion," with "said centralized row-local control portion being physically located inside said image sensor portion in place of a plurality of pixels of the array formed on said image sensor chip," and "thereby forming at least two image sensor areas for each of said at least two CMOS image sensor chips." As noted above in connection with claims 1 and 9, Schick et al. does not teach or suggest an image sensor portion made with "at least two image sensor areas." Heller et al., also having a monolithic image sensor portion, does not cure the deficiencies of Schick et al. Claim 11, and its dependent claim 12, are patentable over the proposed combination of Schick et al. and Heller et al.

Claim 13 recites an image sensor circuit having, *inter alia*, two image sensor chips, each chip having "an image sensor portion having a first area and a second area." As noted above in connection with claims 1, 9, and 11, Schick et al. does not teach or suggest an image sensor portion made with "a first area and a second area." Heller et al. also has a monolithic image sensor portion, and does not cure the deficiencies of Schick et al. Claim 13 is patentable over the proposed combination of Schick et al. and Heller et al.

Claim 17 recites a method of fabricating a CMOS imager that includes, *inter alia*, "forming at least two active image sensor areas in each of said at least two CMOS image sensor chips." Schick et al. does not teach or suggest fabricating a CMOS imager by forming CMOS image sensor chips with "at least two active image sensor areas" as recited in claim 17. Heller et al. also has a monolithic image sensor portion, and does not cure the deficiencies of Schick et al. Claim 17 is patentable over the proposed combination of Schick et al. and Heller et al.

Claims 5 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Schick et al. in view of Heller et al., further in view of U.S. Pat. No. 5,886,353 to Spivey et al. Applicants respectfully request reconsideration of this rejection.

The Office Action requests an explanation of applicants' arguments regarding citation of additional references in the rejection of dependent claims. Applicants agree that the additional citations should not be applied to the independent claims. Applicants did not mean to suggest that the citation of additional references against the dependent claims somehow made the rejection of the independent claim improper. The following remarks have been revised to address the Office Action request for an explanation of Applicants' arguments.

Claim 5 depends from directly from independent claim 1. Claim 1 is patentable over Schick et al. in view of Heller et al. for the reasons advanced above. Spivey et al. has not been cited against claim 1. Even if Spivey et al. had been cited against claim 1, Spivey et al. would not cure the deficiencies of Schick et al. in view of Heller et al. Spivey et al. has been cited as providing interpolation, as noted above. Spivey et al. has a unitary imager portion, and so does not provide the teachings of "a first area and a second area" in the imager portion. Accordingly, claim 1 and dependent claim 5 are patentable over the proposed combination of Schick et al., Heller et al., and Spivey et al.

Claim 12 depends directly from independent claim 11. Claim 11 is patentable over Schick et al. in view of Heller et al. for the reasons advanced above. Spivey et al. has not been cited against claim 11. In any event, Spivey et al. would not cure the deficiencies of Schick et al. in view of Heller et al. Spivey et al. has been cited as providing interpolation of pixels caused by row select logic and spaces between pixel pitches. Spivey et al. has a unitary imager portion, and does not provide the missing teachings of an image sensor portion made with "at least two image sensor areas." Accordingly, claim 11 and dependent claim 12 are patentable over the proposed combination of Schick et al., Heller et al., and Spivey et al.

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schick et al. in view of Heller et al., further in view of U.S. Pat. No. 5,510,623 to Sayag et al. Applicants respectfully request reconsideration of this rejection.

Claim 6 depends directly from claim 1. Claims 1 is patentable over Schick et al. in view of Heller et al. for the reasons advanced above. Sayag et al. has not been cited against claim 1, and even if it had, would not cure the deficiencies of Schick et al. in view of Heller et al. Sayag et al. has been cited as providing row logic in the center of the plurality of pixels. The row logic would create a blind spot in the center of the plurality of pixels. As noted above, however, a primary objective of Schick et al. is to minimize blind spots in the image. The proposed modification of Schick et al. based on Sayag et al. would contradict Schick et al.'s stated objective of minimizing blind spots. There is no motivation in the prior art for such a modification to Schick et al. Instead, it would be counterintuitive, at best, to modify Schick et al. by providing a 'central inactive area' which light would strike. Indeed, Schick et al. teaches directly away from providing the 'central inactive area,' the motivation for which comes only from an improper attempt at hindsight reconstruction of applicants' invention. Claim 1 and dependent claim 6 are patentable over the proposed combination of Schick et al, Heller et al., and Sayag et al.

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schick et al. in view of Heller et al., further in view of U.S. PG PUB 2002/0000549 in the name of Spartiotis et al. Applicants respectfully request reconsideration of this rejection.

Claim 7 depends directly from claim 1. Claim 1 is patentable over Schick et al. in view of Heller et al. for the reasons advanced above. Spartiotis et al. has not been cited against claim 1. Even if Spartiotis et al. had been cited against claim 1, it would not cure the deficiencies of Schick et al. in view of Heller et al. Spartiotis et al. has been cited as providing a guard ring. Spartiotis et al. does not provide the missing "image sensor portion having a first area and a second area," for example. Claim 1 and dependent claim 7 are patentable over Schick et al., in view of Heller et al., further in view of Spartiotis et al.

Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schick et al. in view of Spivey et al. Applicants respectfully request reconsideration of this rejection.

Claim 8 recites a method of capturing an image comprising, *inter alia*, "providing at least two image sensor chips, each chip having first and second parallel edges," and "an image sensor array of imaging pixels that comes within two pixel pitches of said first and second edge," and "includes a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array between said first and second edges." The method also includes "abutting said image sensor chips along at least one of corresponding first and second edges."

Schick et al. discloses a method of capturing an image by providing two image sensor chips each having first and second parallel edges. Schick et al. does not teach or suggest capturing an image by providing two such image sensor chips with "a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array between said first and second edges." Spivey et al. does not cure the deficiencies of Schick et al. Spivey et al. has been cited as providing interpolation that is missing from Schick et al. Spivey et al. discloses overlapping imager chips along lines similar to the chip arrangement in Schick et al. The chips in both Schick et al. and Spivey et al. are overlapped such that active areas block light from impacting the inactive regions. Schick et al. and Spivey et al. teach directly away from including a 'central inactive area' in the image sensor array as described in the Office Action. Thus, Schick et al. and Spivey et al. do not teach providing an image sensor array that "includes a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array between said first and second edges." Claim 8 is patentable over the cited references to Schick et al. and Spivey et al.

In view of the above amendment, applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

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